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SE-6765

B. E. III (Sem. V) (Computer) Examination

April / May – 2011

Microprocessors & Interfacing Techniques

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. 3 (Sem. 5) (Computer)**

Name of the Subject :

☛ **Microprocessors & Interfacing Techniques**

☛Subject Code No. : **6 7 6 5** ☛Section No. (1, 2,.....) : **Nil**

Seat No. :

Student's Signature

1 (a) Answer the following : **10**

(1) The 8085 microprocessor can access memory location upto _____ H.

(2) Mention the number of Machine Cycles & T-states for the 8085 instruction : LXI

(3) Mention the number of Machine Cycles & T-states for the 8085 instruction : RAR.

(4) _____ a logical instruction sets Z(zero) flag, but contents of accumulator are unaffected.

(5) _____ instruction must be used to transfer the contents of accumulator to memory location specified by HL register pair.

(6) Explain the function of pin : RESET OUT

(7) If the result of an arithmetic instruction is 00H in accumulator, the Z(zero) flag=0. [True/False]

(8) If the processor is having 5MHz clock, find out the time required to execute LXI H, 9000H.

(9) In memory mapped I/O, I/O and memory cannot have a same address. Justify.

(10) Why registers are part of microprocessor & not main memory ?

(b) Specify the addressing mode and explain the instructions with example : 4

(a) OUT (b) INX

(c) Answer the following questions : 6

(1) Write a routine HLSP that transfers the contents of SP to HL. No other registers in microprocessor should be affected.

(2) What is shadow memory ?

(3) Explain the function of following routine :

```
LXI SP, 209FH
MVI C, 00H
PUSH B
POP PSW
RET
```

2 (a) Draw and explain timing diagram of the following instruction : 7

C100 : STA 8040H

Opcode of STA : 32H

Draw waveform at all important pins.

(b) Write a program to generate the first 5 elements of fibonacci sequence & store them at locations E000H onwards. (i.e. 1, 1, 2, 3, 5) 8

OR

(b) Write a program equivalent to the following C code : 8

```
for (i = 0; i < 10; i++)
arr[i] = arr[i] * 2;
```

arr is stored at memory location C200H onwards.

3 (a) Interface 16K × 8 EPROM using 4K × 8 chips and one 8255 to 8085. Draw the neat diagram showing the interface scheme and clearly explain the memory map for both devices. Make necessary assumptions and explain with the help of necessary diagrams. 10

(b) Show the contents of all affected registers after execution of each instruction in the following segment of program explain the mathematical function that is performed by the following instructions. **5**

```
MVI A, 07H
RLC
MOV B,A
RLC
RLC
ADD B
```

OR

(b) What is the use of control signals in 8085 ? How control signals are generated ? **5**

4 (a) Answer the following : **10**

(1) Define : Polling.

(2) Define : resolution.

(3) What is the function of cascade lines in 8259 PIC ?

(4) What is functionality of PUSH PSW instruction ?

Give True of False for the following :

(5) RST 5.5 has higher priority than RST 7.5.

(6) RET instruction can be replaced with JMP ADDRESS instruction.

(7) Mode 2 of 8255 is known as bidirectional data transfer mode.

(8) If A0 and A1 are 10 while 8085 is selecting 8255, PORT B of 8255 will be selected.

(9) 8259 has 4 different ICWS.

(10) 8254 timer is 16-bit down timer with 6 operating modes.

(b) Answer the following questions : (Any two) **10**

(1) Explain key debounce techniques.

(2) Explain interrupt acknowledge machine cycle with timing diagram.

(3) Explain with the help of diagram, data transfer during execution of the CALL instruction.

5 (a) Explain with block diagram 8279 programmable keyboard/display interface. **8**

OR

(a) Describe the functions of 8259 programmable interrupt controller with the help of blcok diagram. **8**

(b) Discuss different operating modes of 8255 programmable peripheral interface. **8**

6 (a) Briefly discuss types of communication systems. **10**
Explain 8251 USART with functional block diagram.

(b) Differentiate following with suitable illustration : **4**

(1) Vectored vs. Non-vectored interrupts.

(2) Maskable vs. Non-maskable interrupts.

OR

(b) Draw SIM and RIM instructions' format. **4**
